

October 1987
Revised January 1999

CD4020BC • CD4040BC • CD4060BC
14-Stage Ripple Carry Binary Counters • 12-Stage Ripple Carry Binary Counters • 14-Stage Ripple Carry Binary Counters

General Description

The CD4020BC, CD4060BC are 14-stage ripple carry binary counters, and the CD4040BC is a 12-stage ripple carry binary counter. The counters are advanced one count on the negative transition of each clock pulse. The counters are reset to the zero state by a logical “1” at the reset input independent of clock.

Features

- Wide supply voltage range: 1.0V to 15V
- High noise immunity: 0.45 V_{DD} (typ.)
- Low power TTL compatibility: Fan out of 2 driving 74L or 1 driving 74LS
- Medium speed operation: 8 MHz typ. at V_{DD} = 10V
- Schmitt trigger clock input

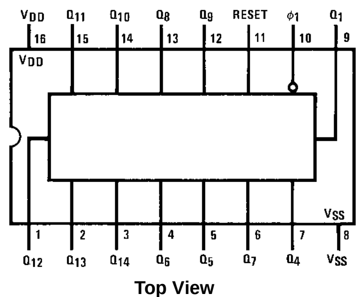
Ordering Code:

Order Number	Package Number	Package Description
CD4020BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150” Narrow
CD4020BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide
CD4040BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150” Narrow
CD4040BCSJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
CD4040BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide
CD4060BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150” Narrow
CD4060BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

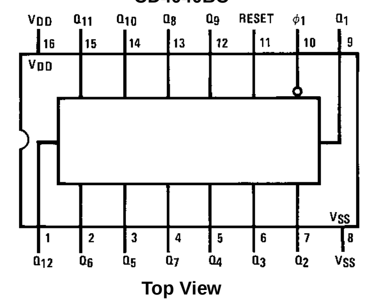
Connection Diagrams

Pin Assignments for DIP and SOIC
CD4020BC



Top View

Pin Assignments for DIP, SOIC and SOP
CD4040BC



Top View

Connection Diagrams (Continued)

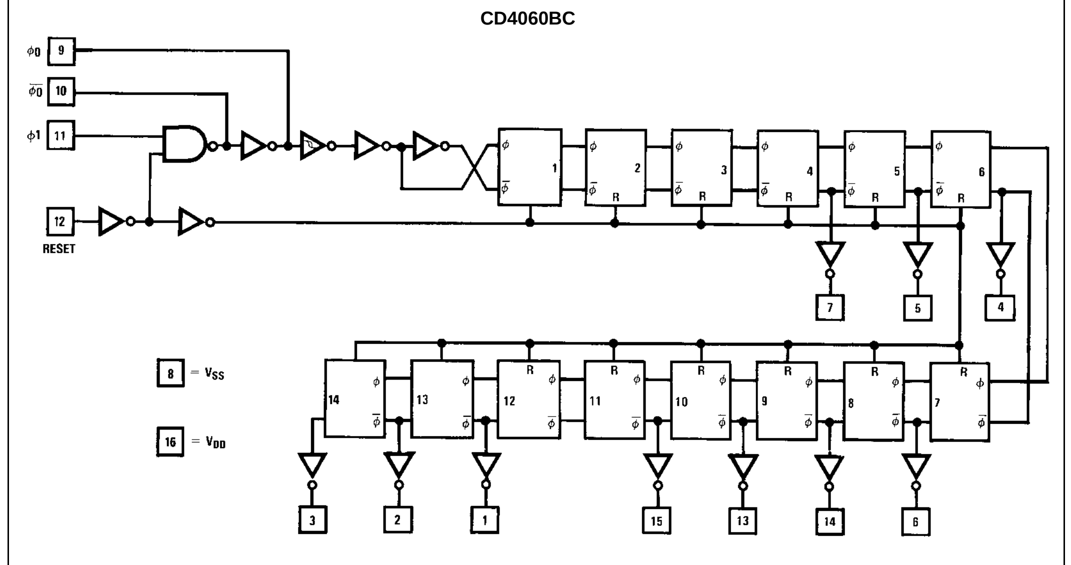
Pin Assignments for DIP and SOIC
CD4060BC

Top View

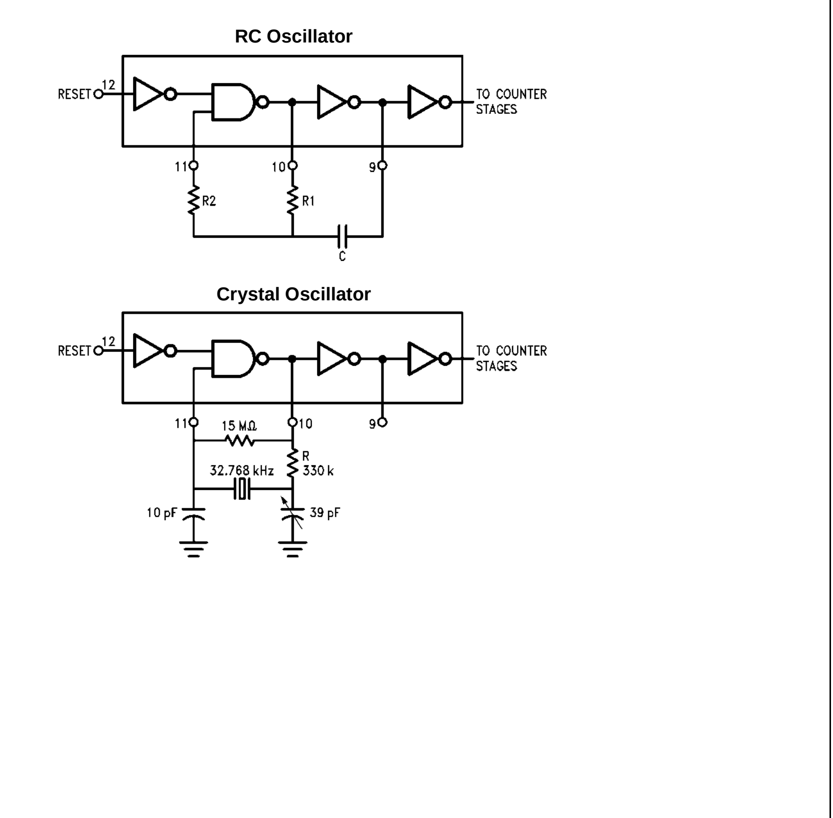
Schematic Diagrams

CD4020BC

CD4040BC



CD4060B Typical Oscillator Connections



Absolute Maximum Ratings (Note 1)

(Note 2)

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to V_{DD} +0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Package Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions

Supply Voltage (V_{DD})	+3V to +15V
Input Voltage (V_{IN})	0V to V_{DD}
Operating Temperature Range (T_A)	−40°C to +85°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20			20		150	µA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40			40		300	µA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80			80		600	µA
V_{OL}	LOW Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	HIGH Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	LOW Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	HIGH Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	LOW Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
	(Note 3)	V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	HIGH Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
	(Note 3)	V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	µA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	µA

Note 3: Data does not apply to oscillator points ϕ_0 and $\overline{\phi}_0$ of CD4060BC. I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics (Note 4)

CD4020BC, CD4040BC $T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, $t_r = t_f = 20$ ns, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL1}, t_{PLH1}	Propagation Delay Time to Q_1	$V_{DD} = 5V$		250	550	ns
		$V_{DD} = 10V$		100	210	ns
		$V_{DD} = 15V$		75	150	ns
t_{PHL}, t_{PLH}	Interstage Propagation Delay Time from Q_n to Q_{n+1}	$V_{DD} = 5V$		150	330	ns
		$V_{DD} = 10V$		60	125	ns
		$V_{DD} = 15V$		45	90	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5V$		125	335	ns
		$V_{DD} = 10V$		50	125	ns
		$V_{DD} = 15V$		40	100	ns
t_{rCL}, t_{fCL}	Maximum Clock Rise and Fall Time	$V_{DD} = 5V$			No Limit	ns
		$V_{DD} = 10V$			No Limit	ns
		$V_{DD} = 15V$			No Limit	ns
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	1.5	4		MHz
		$V_{DD} = 10V$	4	10		MHz
		$V_{DD} = 15V$	5	12		MHz
$t_{PHL(R)}$	Reset Propagation Delay	$V_{DD} = 5V$		200	450	ns
		$V_{DD} = 10V$		100	210	ns
		$V_{DD} = 15V$		80	170	ns
$t_{WH(R)}$	Minimum Reset Pulse Width	$V_{DD} = 5V$		200	450	ns
		$V_{DD} = 10V$		100	210	ns
		$V_{DD} = 15V$		80	170	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance			50		pF

Note 4: AC Parameters are guaranteed by DC correlated testing.

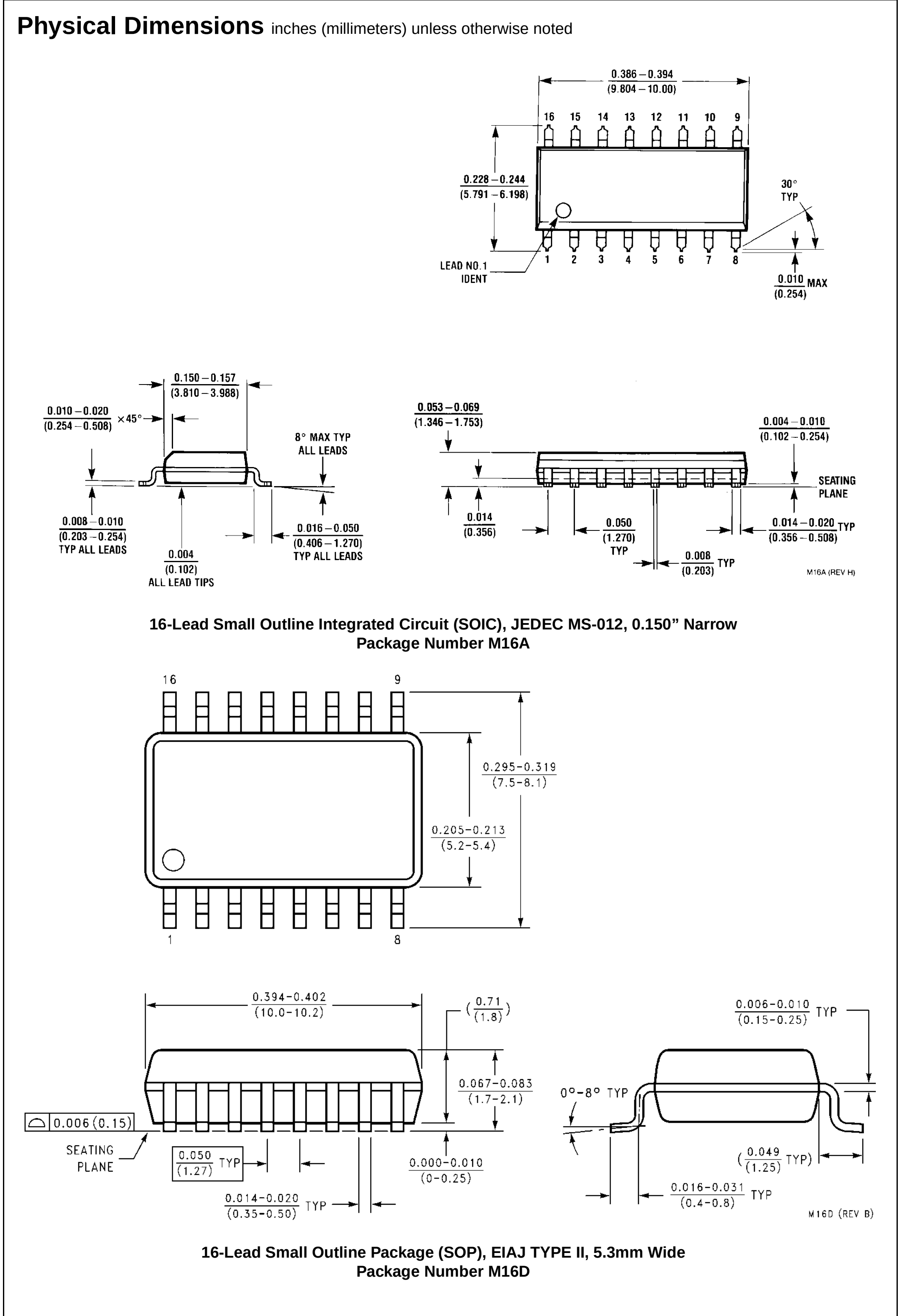
AC Electrical Characteristics (Note 5)

CD4060BC $T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, $t_r = t_f = 20$ ns, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL4}, t_{PLH4}	Propagation Delay Time to Q_4	$V_{DD} = 5V$		550	1300	ns
		$V_{DD} = 10V$		250	525	ns
		$V_{DD} = 15V$		200	400	ns
t_{PHL}, t_{PLH}	Interstage Propagation Delay Time from Q_n to Q_{n+1}	$V_{DD} = 5V$		150	330	ns
		$V_{DD} = 10V$		60	125	ns
		$V_{DD} = 15V$		45	90	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5V$		170	500	ns
		$V_{DD} = 10V$		65	170	ns
		$V_{DD} = 15V$		50	125	ns
t_{rCL}, t_{fCL}	Maximum Clock Rise and Fall Time	$V_{DD} = 5V$			No Limit	ns
		$V_{DD} = 10V$			No Limit	ns
		$V_{DD} = 15V$			No Limit	ns
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	1	3		MHz
		$V_{DD} = 10V$	3	8		MHz
		$V_{DD} = 15V$	4	10		MHz
$t_{PHL(R)}$	Reset Propagation Delay	$V_{DD} = 5V$		200	450	ns
		$V_{DD} = 10V$		100	210	ns
		$V_{DD} = 15V$		80	170	ns
$t_{WH(R)}$	Minimum Reset Pulse Width	$V_{DD} = 5V$		200	450	ns
		$V_{DD} = 10V$		100	210	ns
		$V_{DD} = 15V$		80	170	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance			50		pF

Note 5: AC Parameters are guaranteed by DC correlated testing.

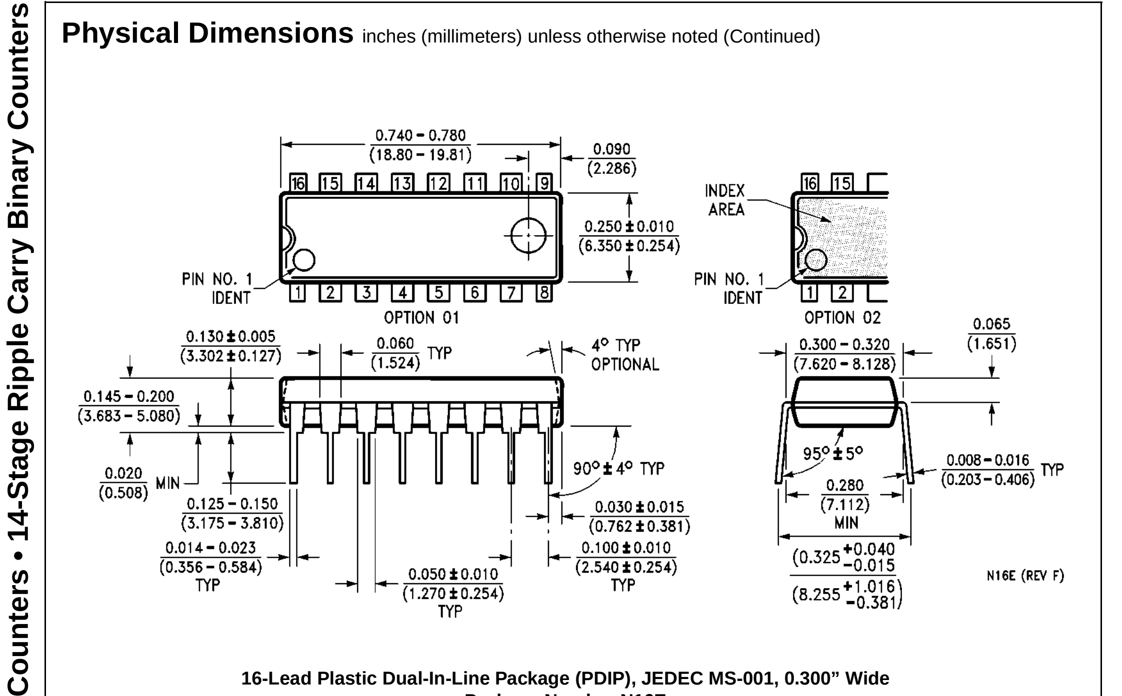
Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150” Narrow
Package Number M16A

16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide
Package Number N16E

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